Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A circuit for detecting an abnormal operation of memory comprising:

a delay circuit for delaying an output data [[of]] output from the memory for a predetermined period of time and for outputting ~~this data as~~ a delayed [[delay]] data responsive thereto; and

a comparison circuit for outputting a noncoincidence ~~an incoincidence~~ signal ~~in case that~~ when the output data output from [[of]] the memory and the [[delay]] delayed data are not coincident with each other ~~after compared~~.

Claim 2 (Currently Amended): A circuit for detecting an abnormal operation of memory according to claim 1 wherein an abnormal operation with regard to an access speed of the memory is detected.

Claim 3 (Currently Amended): A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for holding address information in case of ~~an incoincidence~~ noncoincidence in response to the ~~incoincidence~~ noncoincidence

signal.

Claim 4 (Currently Amended): A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for sounding an alarm when ~~in outputting~~ the ~~incoincidence~~ noncoincidence signal is output.

Claim 5 (Currently Amended): A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for executing an interruption when ~~in outputting~~ the ~~incoincidence~~ noncoincidence signal is output.

Claim 6 (Original): A circuit for detecting an abnormal operation of memory according to claim 1 wherein a delay time of the output data of the memory can be adjusted in the delay circuit.

Claim 7 (Original): A circuit for detecting an abnormal operation of memory according to claim 1 wherein the memory is a flash memory.

Claim 8 (Currently Amended): An integrated circuit comprising ~~a circuit for detecting an abnormal operation of memory according to claim 1~~:

a memory which stores data;

a delay circuit which delays an output data from the memory and outputs a

delayed data responsive thereto; and

a comparison circuit which compares the output data from the memory and the delayed data, and which outputs a noncoincidence signal when the output data and the delayed data are not coincident.

Claim 9 (Currently Amended): A method for detecting an abnormal operation of memory comprising ~~the steps of~~:

delaying an output data output from the [[of]] memory for a predetermined period of time and [[of]] outputting ~~this data as~~ a [[delay]] delayed data responsive thereto; and

outputting ~~an incoincidence~~ a noncoincidence signal ~~in case that~~ when the output data output from [[of]] the memory and the [[delay]] delayed data are not coincident with each other ~~after compared~~.

Claim 10 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 wherein an abnormal operation with regard to an access speed of the memory is detected.

Claim 11 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 further comprising ~~the step of~~ holding address information in case of noncoincidence ~~an incoincidence~~ in response to the ~~incoincidence~~ noncoincidence signal.

Claim 12 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 further comprising ~~the step of~~ sounding an alarm when ~~in outputting~~ the noncoincidence ~~incoincidence~~ signal is output.

Claim 13 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 further comprising ~~the step of~~ executing an interruption [[on]] of a CPU ~~in outputting~~ when the noncoincidence ~~incoincidence~~ signal is output.

Claim 14 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 further comprising ~~the step of~~ rewriting data in [[a]] the memory ~~in outputting~~ when the noncoincidence ~~incoincidence~~ signal is output.

Claim 15 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 wherein a delay time of said ~~the output data of the memory can be adjusted in the~~ delaying [[step]] is adjustable.

Claim 16 (Original): A method for detecting an abnormal operation of memory according to claim 9 wherein the memory is a flash memory.

Claim 17 (New): The integrated circuit according to claim 8, further comprising:

a first latch circuit which stores the output data output from the memory; and

a second latch circuit which stores the delayed data, wherein the comparison circuit receives the output data stored in the first latch circuit and the delayed data stored in the second latch circuit.

Claim 18 (New): The integrated circuit according to claim 8, further comprising an address information storing circuit which stores an address information when the comparison circuit outputs the noncoincidence signal.